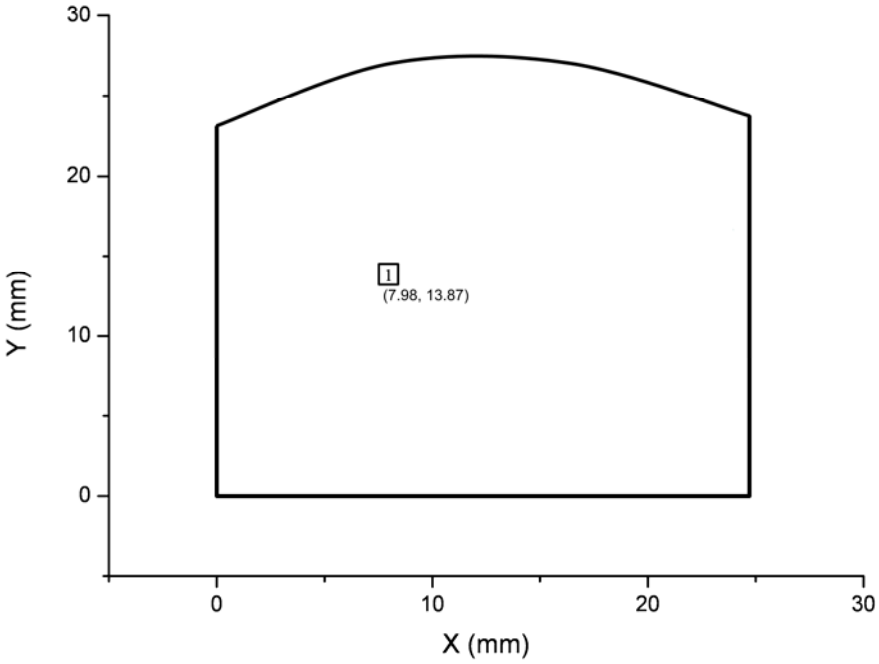
LRW-0021 Datasheet

Parent Wafer

Si Orientation	<100>
Si Thickness	500-560µm
Resistivity	0.001-0.005Ωcm
Oxide	300nm Dry Thermal Oxide

Substrate Map



Flake 1: x=7.98mm, y=13.87mm Area: >**30000µm^2** (**single layer**)