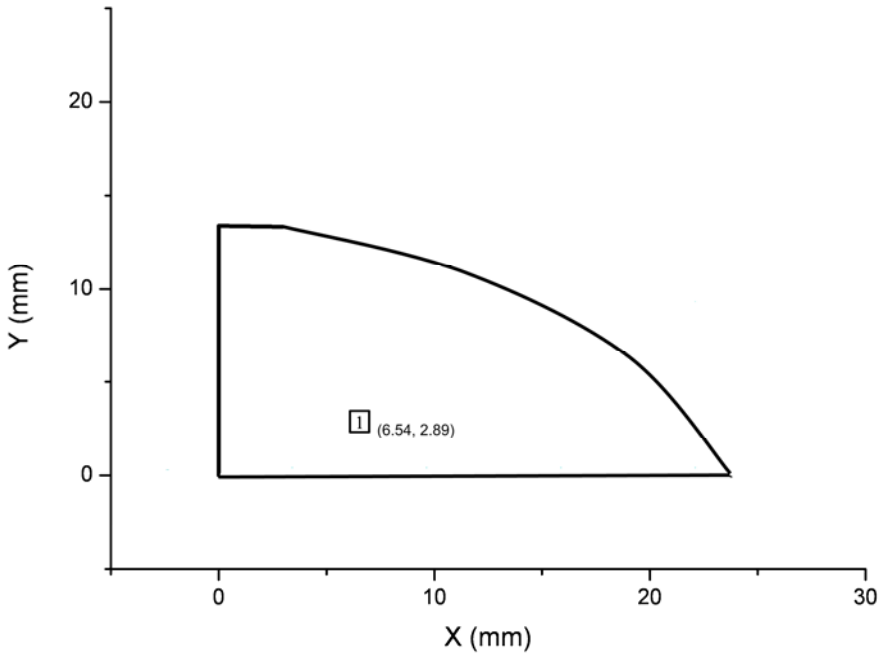
LRW-0026 Datasheet

Parent Wafer

Si Orientation	<100>
Si Thickness	500-560µm
Resistivity	0.001-0.005Ωcm
Oxide	300nm Dry Thermal Oxide

Substrate Map



Flake 1: x=6.54mm, y=2.89mm Area: >135000µm^2 (three layers)