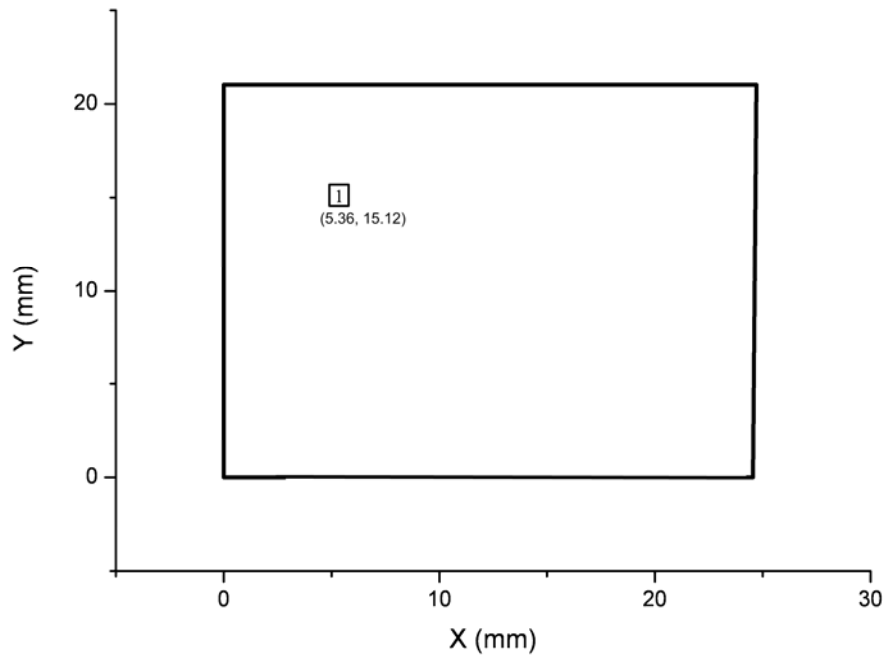


# LRW-0060 Datasheet

## Parent Wafer

<b>Si Orientation</b>	<100>
<b>Si Thickness</b>	500-560 $\mu$ m
<b>Resistivity</b>	0.001-0.005 $\Omega$ cm
<b>Oxide</b>	300nm Dry Thermal Oxide

## Substrate Map



**Flake 1:** x=5.36mm, y=15.12mm Area: >6800 $\mu\text{m}^2$  (single layer)

