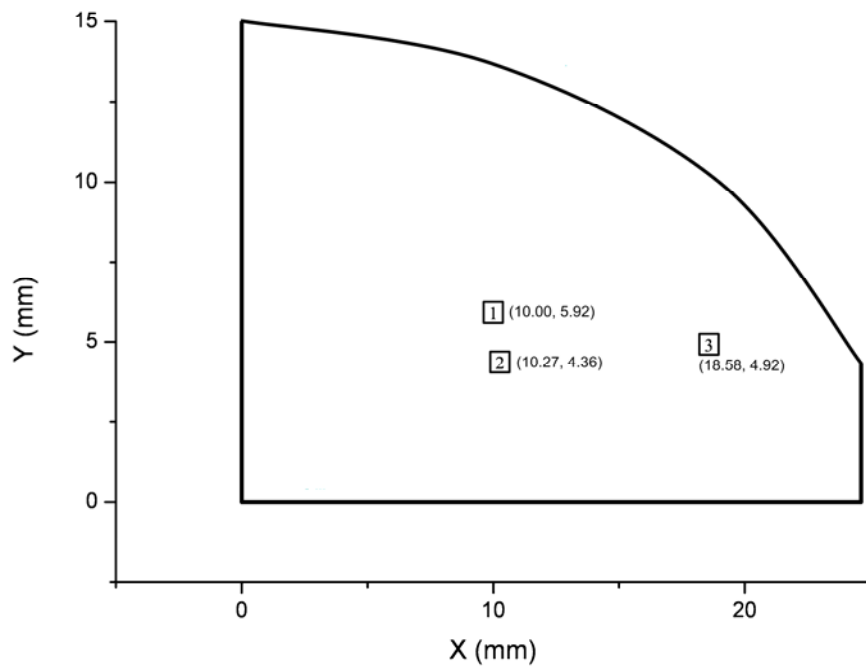


# LRW-0064 Datasheet

## Parent Wafer

<b>Si Orientation</b>	<100>
<b>Si Thickness</b>	500-560 $\mu$ m
<b>Resistivity</b>	0.001-0.005 $\Omega$ cm
<b>Oxide</b>	300nm Dry Thermal Oxide

## Substrate Map



**Flake 1:** x=10.00mm, y=5.92mm Area: >95000 $\mu\text{m}^2$  (single layer)



**Flake 2:** x=10.27mm, y=4.36mm

Area: A>86000 $\mu\text{m}^2$  (single layer) B>80000 $\mu\text{m}^2$  (single layer)





**Flake 3:** x=18.58mm, y=4.92mm Area: >31000 $\mu\text{m}^2$  (single layer)

